

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT**  
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.  
SC12042ZK

In Re Application:

Wang et al.

Serial No.  
Unknown

Filing Date

Examiner  
Unknown

Group Art Unit  
Unknown

**SEMICONDUCTOR DEVICE WITH STRAIN RELIEVING BUMP DESIGN**

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(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

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Dated: July 31, 2003

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Docket No.  
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07/31/2003

Examiner  
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Title:

**SEMICONDUCTOR DEVICE WITH STRAIN RELIEVING BUMP DESIGN**

Address to:  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**37 CFR 1.97(b)**

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

**37 CFR 1.97(c)**

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

☐ the statement specified in 37 CFR 1.97(e);

**OR**

☐ the fee set forth in 37 CFR 1.17(p).

<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>		Docket Number (Optional) <b>SC12042ZK</b>		Application Number <b>Unknown</b>	
		Applicant(s) <b>Wang et al.</b>			
		Filing Date <b>July 31, 2003</b>		Group Art Unit <b>Unknown</b>	
<b>*EXAMINER INITIAL</b>	<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>				
	1	John C. Carson, "Advances in Chip Level Packaging" (2002 Lecture notes, Johns Hopkins University)			
	2	"MicroPro Proves Effective for uBGA Sphere Attach", Speedline (a publication of Speedline Technologies), Issue #2 (Summer 2001)			
	3	D. Light, D. Castillo, M. Beroz, M. Nguyen, and T. Wang, "Vertical Expansion (WAVE) Packaging Process Development" (published by Tessera Technologies, 2001)			
	4	Joseph Fjelstad, "Strategies for Creating Compliant IC Packages at Near Chip Size" (INTERPACK 1999)			
	5	K. Klein, T. Leichle, E. Moss, P. Sassone and X. Wei, "A Survey of Compliant Interconnects for Wafer Level Packaging" (December 13, 2001)			
<b>EXAMINER</b>		<b>DATE CONSIDERED</b>			
<b>*EXAMINER:</b> Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					